

A Survey on Analog Testing Methodologies

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ABSTRACT: Analog circuit testing is considered to be a very complex task, primarily to the lack of fault models and accessibility to internal nodes. Conventionally, work on analog testing has focused on analysis of faults in board designs. Recently, with increasing levels of integration, not just diagnosing faults, but distinguishing between faulty and a fault free circuit has become a big challenge. The complexity of today's analog circuits and their many parameters, as well as the restricted accessibility to their internal modules, restricts the use of conventional automatic test equipment. Such equipment does not have enough storage and lacks the capability of computation during actual testing. Various papers have proposed different techniques to reduce the burden of testing analog circuits. This survey attempts to outline some of the work, providing different methodologies used to test an Analog circuit.

Key words: Analog Circuits, Analog Testing and Analog Fault Analysis

I. INTRODUCTION

Analog circuits are a superior class of circuits, in that, they include all continuous time, continuous-amplitude signal processing circuits. Examples include dc power supply circuits such as regulators, op- amps, and signals conditioning circuits. Analog circuits have their input and output both as continuous- in- time and continuous –in-amplitude.

Digital circuits have both their inputs and outputs in the discrete-time discrete-amplitude domain.

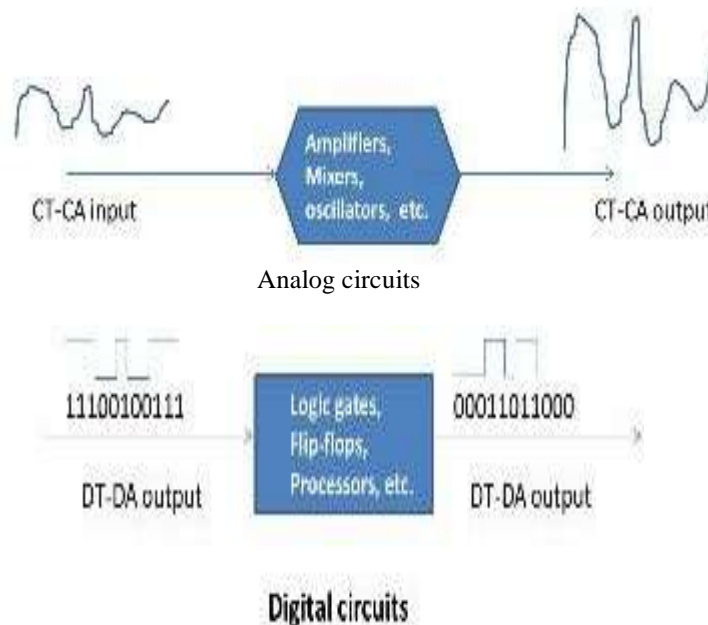


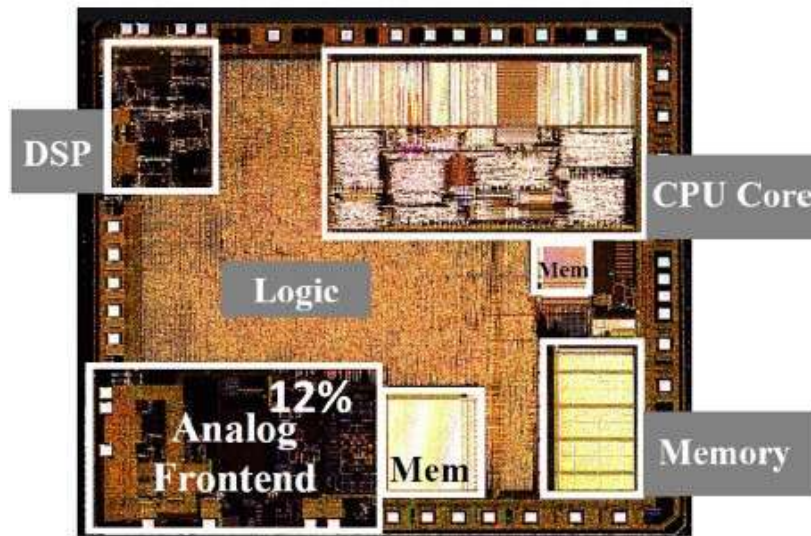
Figure 1 Distribution of input/output functions in analog and digital circuits

II. COMPARATIVE STUDY ON ANALOG TEST AND DIGITAL TEST

Digital circuits have concise fault models (such as stuck-at fault) allowing the use of “structural” tests which intend specific faults instead of testing for the entire functionality of the circuit. Consider a combinational digital circuit with ‘n’ inputs, then the number of test vectors needed to test that circuit will be 2^n . In contrast, analog circuits propagate signals through them in a range of signal values, requiring a large number of test signals to test the circuit. The faulty analog circuit (with an unexpected behavior) can take a whole range of incorrect values.

A large number of fault-injections may be required to model a fault even at a single node of an analog circuit. This difficulty of fault models makes the model-based testing of analog circuits an unsuitable proposition. To test the functionality of the circuit, a large set of signals are used in common in industry.

Figure 1.2 Mixed-signal System-on-Chip (SoC) showing size of analog block as a fraction of total die area.



Analog interface contributes to about 12% of the total die area [1].

Furthermore, though analog circuits contribute less than 10-20% of the chip area, they account for over 50% of the test cost [2].

III. ANALOG TEST AND DIAGNOSIS

The Research focus is mainly in the diagnosis of identifying a faulty component in the circuit, so that the faulty component can be replaced in order to avoid an unacceptable deviation in the output.

1.1. Taxonomy of Analog Circuit Fault-Diagnosis Techniques

Faults in analog circuits can be classified as catastrophic and parametric. Catastrophic faults are open and short circuits, caused by sudden and large variations of components. We define parametric faults based on the circuit's functionality. Here, the value of a parameter deviates continuously with time or with environmental conditions to an unacceptable value. In analog circuits, the interest is the selection of parameters to be assayed, and the verity to which they should be tested, to detect the aberration of faulty components. In general, analog circuit testing has three objectives: detection, location, and identification (diagnosis). Fault detection is a minimum requirement. Fault location is necessary for repairing faulty parts at a later time. Fault identification is required for adjustment or tuning, for which we must know the exact value of the deviations [3].

A number of different standards could be used for categorizing fault-diagnosis techniques. The common method of assortment is based on the stage in the testing at which simulation of the circuit is undertaken [4,5,6]: Simulation-before-test, and Simulation-after-test. The following figure shows the various methods used in fault diagnosis.

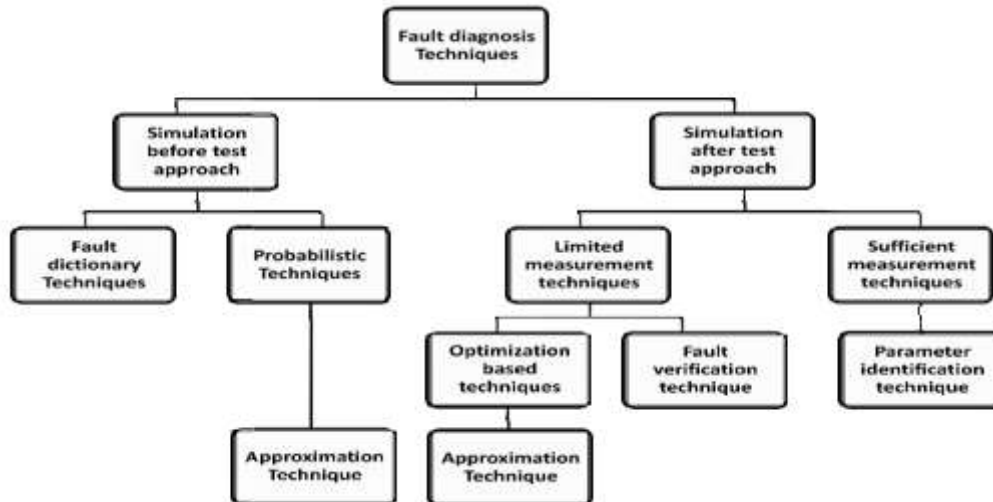


Figure 1.3 Classification of fault diagnosis techniques []

Simulation-Before-Test

Simulation-before-test approaches commence with a fault list. The faults are then simulated to determine the equivalent responses to predetermined stimuli. Faults are accordingly diagnosed by comparing simulated and observed responses. Simulation-before-test algorithms are based on a fault dictionary.

In specific, the most likely faults (usually catastrophic) are predicted based on a fault model and a set of input stimuli and measurements are selected to detect faults. The computations may be dc responses, ac responses at circuit outputs, ac responses at the power supply node, transient responses at circuit outputs, or transient responses at the power supply node. Then for these set of potential faults, the circuit's response for each stimulus is evaluated for each fault with all but the faulty parameter set to nominal values, i.e., the parameters for which the circuit was designed. The responses for each fault are typically evaluated using circuit simulation, except for the special case when the circuit is linear, where efficient techniques exist for computing the faulty responses. After evaluating the responses corresponding to the faults, the faults and their corresponding responses are stored in a dictionary. To diagnose a fault, the measurements of the circuit being tested are compared with measurements in the dictionary. The fault is identified by determining the nearest simulated fault using examination [8].

Simulation-After-Test

Simulation-after-test approaches, however, begin with the unsuccessful responses, which are then used to evaluate faulty parameter or component values. Simulation-after-test algorithms have been designed to figure out for values of component characteristics, given a set of measured responses and knowledge of the circuit topology. A fault is identified if one or more parameter values are found to be outside of tolerance. Hence a fault can be detected if it is possible to uniquely solve for all characteristics from the given measurements [8].

1.2. In circuit testing and Functional testing

Initial methods of analog testing are In-circuit testing and functional testing. The in circuit approach tests for digital circuits along with analog circuits and electrically separates the components to be tested from all other components associated to them. It tests them independently to determine their functionality. Maximum in-circuit testing system use operational amplifier which is circumscribed in its capacity to function at high frequency. The in-circuit technique becomes very difficult for complex circuits, which require hundreds of test pins and where access to the components' connections becomes increasingly difficult. With this technique, the function of the complete circuit is not tested.

Functional testing is based on the verification of a circuit's functionality by applying stimuli signals at the input and verify its outputs. This type of test is convenient for complex analog circuits. Its major disadvantage is difficulty in detecting and identifying the defective elements and complexity in writing the test programs [3].

1.3. System level testing using correlation functions

The proposed testing method is based on the excitation of the analog circuit being tested with a sequence of pulses, and subsequent comparison of the captured circuit response with a signature of the known fault-free response. In the proposed test method the type of test sequence to be applied to an analog circuit in a mixed-signal IC is a PRBS (pseudorandom binary sequence). The PRBS is chosen because it can be easily

generated, it is compatible with digital BIST circuitry, Such sequences have well defined properties and can be used to estimate the impulse response of the analog circuit under test (CUT)[9].

The transient response data captured at the output of an analog CUT is analyzed to determine if the fault has been detected or not. The detection method used in this paper is based on comparing the signatures of the autocorrelation and cross-correlation functions of the fault free circuit with those of the CUT. A tolerance window is placed around the said functions of the fault-free circuit to take care of acceptable deviation in the circuit output voltage from the ideal response. Single catastrophic and soft fault conditions are introduced to the CUT and the auto and cross correlation functions are computed and compared with those of the tolerated fault-free circuit. If either of the correlation function of the CUT generates a signature that falls outside the boundaries of the tolerance window of the corresponding fault-free correlation function on at least one instant, then that fault is considered detectable[9].

1.4. Testing of Analog circuits using spectralanalysis

In this method, power spectral density (PSD) is considered to have enough information to work as a digital signature. The basic idea is shown in Fig. 2. In the training phase, a random noise with known statistical characteristics is applied to the input of the fault-free circuit, and the PSD of the output is estimated. This is kept as the signature of the fault-free circuit. In the testing phase, the PSD of the circuit under test (CUT) is estimated and compared to the signature of the fault-freecircuit.

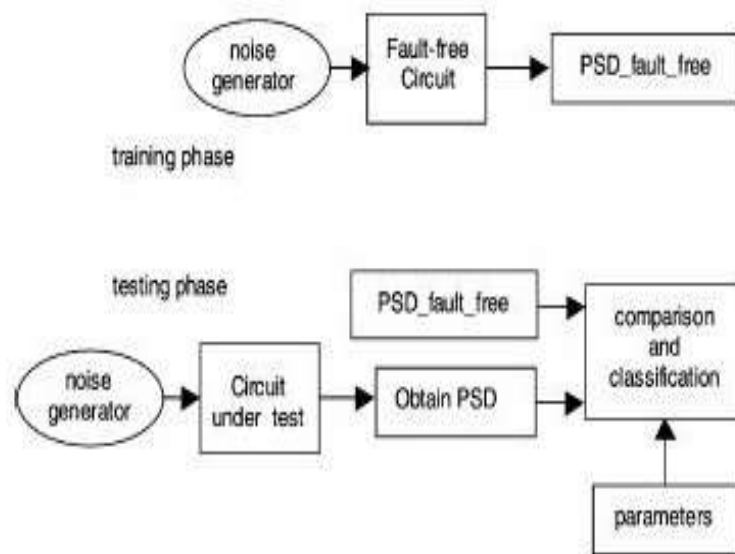


Figure 2 Testing using power spectral density estimation [10]

The technique is able to detect deviations in the transfer function of a system using the PSD as a basic signature. A distance is evaluated between the faulty and faulty-free PSD. If a given analog circuit has a very low sensitivity to one, then the transfer function will have a small deviation from the faulty free case. On the other hand, if the sensitivity is high, even small component variations would produce large deviations in the PSD from the faulty free case. The drawback is that the PSD estimate will have a lower frequency resolution, and this could mask the presence of soft deviations in the CUT [10].

1.5. Testing of Analog circuits using Transient outputvoltage

In this method, the transient output voltage of analog circuits was used for fault detection. The circuits were stimulated by a transient signal source. It's transient output voltage was measured and analyzed. Then the features of this signal are extracted. Principal component analysis was used to combine these features and detect faults of circuits-under-test. It can used both in time domain and the features in frequency domain simultaneously. The selected features of transient output voltage signal are: the magnitude component values of the first four harmonics in frequency domain, the peak to peak value, the maximum value, the standard deviation, and the mean value in time domain. The transient output voltages of CUT are analyzed by these eight features. At first, the principal component model of fault-free circuits are constructed. This model is constructed according to the features of transient output voltage in fault-free circuits. So, this model can be used to detect faults of circuits under test. If the CUT is faulty, the relations of features will be disturbed. They will be different with those in fault-free circuits[11].

1.6. Testing of Analog circuits using sensitivity analysis

Sensitivity gives a scale of the circuit's performance change in response to a change in the circuit elements values. A good electrical circuit design requires the use of optimization methods to improve the circuit's performance by using the sensitivity analysis. The sensitivity determination is a classical approach that has most often been used to examine the performance of circuits. Deviation from the nominal elements values can distort the response and result in an undesirable or unstable circuit. Sensitivity is defined as the effect of a change in the element x to the resulting change in the circuit performance parameters T . Differential sensitivity is defined as the change of the output parameters T due to an infinitesimal change of the element x ($\Delta x \rightarrow 0$). The following equation defines the differential sensitivity of parameter T_j with respect to component X_i .

$$S_{T_j}^{X_i} = \frac{\Delta T_j}{T_j} \bigg/ \frac{\Delta X_i}{X_i} \quad (1)$$

when the element x is submitted to a large perturbation or deviation, the resulting change in the output parameter T is analyzed by the incremental sensitivity. The subsequent equation defines the incremental sensitivity

$$q_{T_j}^{X_i} = \frac{\Delta T_j}{\Delta X_i} \quad (2)$$

where ΔT_j is the variation in parameter T_j resulting from an incremental variation in component X_i . The above approach in an algorithmic way is as follows:

- Acquiring the parameters and the components' actual values from the good circuit.
- Estimation of the response parameters of the faulty circuit.
- Calculating of the sensitivity of the output parameters.
- Calculation of the sensitivities at the definite values of the components
- From the above assessment, formation of Equation 1 and 2.
- Determination of the results $(\Delta x_i) / x_i$ of the system.

If the desired degree of precision is obtained, the algorithm ends [3].

IV. CONCLUSION

The methodologies to test Analog circuits have been discussed. Each method has its own advantages. As testing is significant with which analysis on Analog faults can be performed. Fault detection and fault identification can also be implemented by using any one of the above suitable methods. The above methods can be combined as required to perform testing of analog, digital and mixed signal circuits.

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